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The Design of the Seer Predictive Caching System - Kuenning (1994) (Correct) (41 citations)
The Design of the Seer **Predictive Caching** System Geoffrey H. Kuenning Computer
complex and deliberately hidden. Seer is a **predictive caching** system that observes user behavior, makes
ftp.cs.ucla.edu/pub/ficus/mcsa94.ps.gz

Predicting File System Actions from Prior Events - Kroeger, Long (1996) (Correct) (40 citations)
we have transformed an LRU cache into a **predictive cache** that in our simulations averages 15% more
LRU. In fact, on average our fourmegabyte **predictive cache** has a higher cache hit rate than a 90
csl.cse.ucsc.edu/reports/../papers/usenix-96.ps

Intelligent File Hoarding for Mobile Computers - Tait, Lei (1995) (Correct) (26 citations)
[7] uses a method for transparent hoarding (**predictive caching**"that is based on the notion of semantic
[7] G. H. Kuenning. The Design of the Seer **Predictive Caching** System. In IEEE Workshop on Mobile
www-2.cs.cmu.edu/afs/cs.cmu.edu/user/satya/Web/MCSALINK/PAPERS/tait95.pdf

Partially Connected Operation - Huston, Honeyman (1995) (Correct) (24 citations)
support for low bandwidth networks, such as **predictive caching** to obviate network demands caused by cache
www.citi.umich.edu/u/homey/papers/pco.cs.PS

Seer: Predictive File Hoarding for Disconnected Mobile Operation - Kuenning (1997) (Correct) (18 citations)
: 103 9.1.1 **Predictive Caching** :
behavior that supports the hypothesis that **predictive caching** is a feasible method of managing data on a
ftp.cs.ucla.edu/tech-report/97-reports/970015.ps.Z

Improving File System Performance via Predictive Caching - James Griffioen (1995) (Correct) (5 citations)
Improving File System Performance via **Predictive Caching** James Griffioen, Randy Appleton
Improving File System Performance via **Predictive Caching** Abstract Despite impressive advances in
casaturn.kaist.ac.kr/~sikang/course/CS530/GA95.ps.gz

File Access Prediction with Adjustable Accuracy - Ahmed Amer Darrell (2002) (Correct) (4 citations)
avoids the timeliness requirements of **predictive caching**, and yet is dependent on the quality and
www.cs.uh.edu/~paris/MYPAPERS/ipccc02.pdf

The Persistent Relevance of the Local Operating System to Global.. - Lepreau (1996) (Correct) (4 citations)
to implement and reaps large benefits [18]**predictive caching** based on historical access patterns [20]
mancos.cs.utah.edu/papers/dist-vs-local.ps.Z

Predicting File System Actions From Reference Patterns - Kroeger (1996) (Correct) (2 citations)
with a predictive prefetcher, creating a **predictive cache** that, in our simulations, averages 14% more
We show that on average our four megabyte **predictive cache** has a higher cache hit ratio than a 90
csl.cse.ucsc.edu/~tmk/publications/masters/masters.ps

PROMISE: Predicting Query Behavior to Enable Predictive.. - Carsten Sapia Forwiss (2000) (Correct)
(1 citation)
PROMISE: Predicting Query Behavior to Enable **Predictive Caching** Strategies for OLAP Systems 1 Carsten
Design, Implementation, and Evaluation of a **Predictive Caching** File System, Technical Report No.
www.forwiss.tu-muenchen.de/~system42/publications/dawak00_camweb.pdf

Performance Impact of Proxies in Data Intensive.. - Beynon, Sussman, Saltz (1999) (Correct) (1 citation)
a proxy to perform various functions such as **caching, predictive** Backend Frontend Backend Client QBatch
www.cs.umd.edu/users/beynon/papers/ics99.ps.Z

Data Management for User Profiles in Wireless.. - Jannink, Lam.. (1995) (Correct) (1 citation)
also maintain mobility patterns of users for **predictive caching** and replication [SW95]3. Feature Support
www-db.stanford.edu/pub/papers/profile.ps

File System Support for Weakly Connected Operation - Kevin Froese (1995) (Correct) (1 citation)
in the cache [14]and through long-term **predictive caching** techniques [3, 7]While operating in
[7] Kuenning, G. The design of the seer **predictive caching** system. In Workshop on Mobile Computing
www.cs.usask.ca/staff/kwf230/research/880_Paper.ps.gz

Acceleration of Mobile Commerce using Predictive - Retrieval Amund Tveit (2002) (Correct)
caching, and Fireclick Inc. for "last mile" **predictive caching**)The party who pays for these services is
www.idi.ntnu.no/~amundt/publications/2002/MobAccelerationPaper.pdf

European Commission - Directorate General Jrc (Correct)
many techniques for managing such a cache (**predictive caching**, off-line synchronization and replication
available many techniques for managing such a cache (**predictive caching**, off-line synchronization and
infoweb.jrc.it/kotsakis/publications/../publications/reports/SAINT-Preliminary-Design.pdf

System Support for Mobile Wireless Computing - Pitoura (Correct)
5 DO in File Systems #Seer #46# **predictive caching** scheme: les are automatically prefetched
#46# G. H. Kuenning. The Design of the Seer **Predictive Caching** System. In Proceedings of the IEEE
www.cs.vt.edu/~irchen/6204/pdf/chap3.pdf

Cache Management for Mobile File Service - Froese, Bunt (Correct)
in the cache [7]and applying long-term **predictive caching** techniques [8, 9]For weakly connected
[9] G. Kuenning. The design of the Seer **predictive caching** system. In Proc. Workshop on Mobile
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Improving Performance On WWW Using Path-Based Predictive Caching.. - Zhang (2001) (Correct)
Improving Performance On Www Using Path-Based **Predictive Caching** And Prefetching By Haining Zhang
B.sc.
Performance on WWW Using Path-based **Predictive Caching** and Prefetching Examining Committee: Dr.
fas.sfu.ca/pub/cs/theses/2001/HainingZhangMSc.ps.gz

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1 Prediction caches for superscalar processors
James E. Bennett, Michael J. Flynn
December 1997 **Proceedings of the 30th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.02 MB) Additional Information: full citation, abstract, references, index terms
Publisher Site

Processor cycle times are currently much faster than memory cycle times, and this gap continues to increase. Adding a high speed cache memory allows the processor to run at full speed, as long as the data it needs is present in the cache. However, memory latency still affects performance in the case of a cache miss. Prediction caches use a history of recent cache misses to predict future misses and to reduce the overall cache miss rate. This paper describes several prediction caches, and introdu ...

Keywords: Dynamic scheduling, Memory latency, Stream buffer, Victim cache, Prediction cache

2 Predictive caching strategy for on-demand routing protocols in wireless ad hoc networks
Wenjing Lou, Yuguang Fang
November 2002 **Wireless Networks**, Volume 8 Issue 6
Full text available: pdf(221.65 KB) Additional Information: full citation, abstract, references, citings, index terms

Route caching strategy is important in on-demand routing protocols in wireless ad hoc networks. While high routing overhead usually has a significant performance impact in low bandwidth wireless networks, a good route caching strategy can reduce routing overheads by making use of the available route information more efficiently. In this paper, we first study the effects of two cache schemes, "link cache" and "path cache", on the performance of on-demand routing protocols through simulations base ...

Keywords: ad hoc networks, dynamic source routing, on-demand routing, timeout mechanism

3 Special issue on ICML: Learning to construct fast signal processing implementations
Bryan Singer, Manuela Veloso

March 2003 **The Journal of Machine Learning Research**, Volume 3

Full text available: pdf(5.52 MB) Additional Information: full citation, abstract, index terms

A single signal processing algorithm can be represented by many mathematically equivalent formulas. However, when these formulas are implemented in code and run on real machines, they have very different runtimes. Unfortunately, it is extremely difficult to model this broad performance range. Further, the space of formulas for real signal transforms is so large that it is impossible to search it exhaustively for fast implementations. We approach this search question as a control learning problem ...

4 Way-predicting set-associative cache for high performance and low energy consumption

Koji Inoue, Tohru Ishihara, Kazuaki Murakami

August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**

Full text available: pdf(375.17 KB) Additional Information: full citation, references, citings, index terms

5 Memory hierarchies: Direct load: dependence-linked dataflow resolution of load address and cache coordinate

Byung-Kwon Chung, Jinsuo Zhang, Jih-Kwon Peir, Shih-Chang Lai, Konrad Lai

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings

Publisher Site

An increasing cache latency in future processors incurs profound performance impacts in spite of advanced out-of-order execution techniques. In this paper, we describe an early address resolution mechanism that accurately resolves both regular and irregular load addresses. The basic idea is to build dynamic dependence links from the instruction that updates the base register to the consumer load instructions. Once a new base address is available, it triggers calculations of the new load addresse ...

6 Simultaneous subordinate microthreading (SSMT)

Robert S. Chappell, Jared Stark, Sangwook P. Kim, Steven K. Reinhardt, Yale N. Patt

May 1999 **ACM SIGARCH Computer Architecture News , Proceedings of the 26th annual international symposium on Computer architecture**, Volume 27 Issue 2

Full text available: pdf(129.54 KB) Additional Information: full citation, abstract, references, citings, index terms

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Current work in Simultaneous Multithreading provides little benefit to programs that aren't partitioned into threads. We propose Simultaneous Subordinate Microthreading (SSMT) to correct this by spawning subordinate threads that perform optimizations on behalf of the single primary thread. These threads, written in microcode, are issued and executed concurrently with the primary thread. They directly manipulate the microarchitecture to improve the primary thread's branch prediction accuracy, cac ...

7 Embedded systems: applications, solutions and techniques (EMBS): An energy efficient cache memory architecture for embedded systems

Park Jung-Wook, Kim Cheong-Ghil, Lee Jung-Hoon, Kim Shin-Dug

March 2004 **Proceedings of the 2004 ACM symposium on Applied computing**

Full text available: pdf(277.70 KB) Additional Information: full citation, abstract, references, index terms, review

This paper proposes a modified two-way set associative cache for embedded systems to

reduce the energy consumption. For this goal, the proposed cache, called SSA (selective-way-access skewed associative) cache, equips with a way-selecting mechanism controlled by skewing function and small table look-up, which also has the reconfigurable ability to be converted to one direct mapped cache on a specific application. The skewing mechanism including differentiated mapping function for each cache set, ...

Keywords: embedded system, low power cache, memory hierarchy, selective way access, skewed associativity

8 Difficult-path branch prediction using subordinate microthreads

Robert S. Chappell, Francis Tseng, Adi Yoaz, Yale N. Patt

May 2002 **ACM SIGARCH Computer Architecture News**, Volume 30 Issue 2

Full text available: pdf(1.14 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Branch misprediction penalties continue to increase as microprocessor cores become wider and deeper. Thus, improving branch prediction accuracy remains an important challenge. Simultaneous Subordinate Microthreading (SSMT) provides a means to improve branch prediction accuracy. SSMT machines run multiple, concurrent microthreads in support of the primary thread. We propose to dynamically construct microthreads that can speculatively and accurately pre-compute branch outcomes along frequently mis ...

Keywords: high performance microprocessor, branch prediction, SSMT, SMT, helper thread, microarchitecture, microthread

9 Information Retrieval: Predictive caching and prefetching of query results in search engines

Ronny Lempel, Shlomo Moran

May 2003 **Proceedings of the 12th international conference on World Wide Web**

Full text available: pdf(212.73 KB) Additional Information: full citation, abstract, references, citings, index terms

We study the caching of query result pages in Web search engines. Popular search engines receive millions of queries per day, and efficient policies for caching query results may enable them to lower their response time and reduce their hardware requirements. We present PDC (probability driven cache), a novel scheme tailored for caching search results, that is based on a probabilistic model of search engine users. We then use a trace of over seven million queries submitted to the search engine A ...

Keywords: caching, query processing and optimization

10 Caching: Efficient prediction of web accesses on a proxy server

Wenwu Lou, Hongjun Lu

November 2002 **Proceedings of the eleventh international conference on Information and knowledge management**

Full text available: pdf(350.55 KB) Additional Information: full citation, abstract, references, index terms

Web access prediction is an active research topic with many applications. Various approaches have been proposed for Web access prediction in the domain of individual Web servers but they have to be tailored to the domain of proxy servers to satisfy its special requirements in prediction efficiency and scalability. In this paper, the design and implementation of proxy-based prediction service (PPS) is presented. For prediction efficiency, PPS applies a new prediction scheme which employs a two-la ...

Keywords: navigational model, proxy server, web access prediction

11 Mining web logs for prediction models in WWW caching and prefetching
Qiang Yang, Haining Henry Zhang, Tianyi Li
August 2001 **Proceedings of the seventh ACM SIGKDD international conference on Knowledge discovery and data mining**
Full text available: pdf(413.83 KB) Additional Information: full citation, abstract, references, citings, index terms

Web caching and prefetching are well known strategies for improving the performance of Internet systems. When combined with web log mining, these strategies can decide to cache and prefetch web documents with higher accuracy. In this paper, we present an application of web log mining to obtain web-document access patterns and use these patterns to extend the well-known GDSF caching policies and prefetching policies. Using real web logs, we show that this application of data mining can achieve dr ...

Keywords: Application to Caching and Prefetching on the WWW, Web Log Mining

12 Improving CISC instruction decoding performance using a fill unit
Mark Smotherman, Manoj Franklin
December 1995 **Proceedings of the 28th annual international symposium on Microarchitecture**
Full text available: pdf(965.34 KB) Additional Information: full citation, references, citings, index terms

13 Hardware-driven prefetching for pointer data references
Chi-Hung Chi, Chin-Ming Cheung
July 1998 **Proceedings of the 12th international conference on Supercomputing**
Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

14 The cache performance and optimizations of blocked algorithms
Monica D. Lam, Edward E. Rothberg, Michael E. Wolf
April 1991 **Proceedings of the fourth international conference on Architectural support for programming languages and operating systems**, Volume 19 , 25 , 26 Issue 2 , Special Issue , 4
Full text available: pdf(1.20 MB) Additional Information: full citation, references, citings, index terms

15 Coupling compiler-enabled and conventional memory accessing for energy efficiency
Raksit Ashok, Saurabh Chheda, Csaba Andras Moritz
May 2004 **ACM Transactions on Computer Systems (TOCS)**, Volume 22 Issue 2
Full text available: pdf(1.41 MB) Additional Information: full citation, abstract, references, index terms

This article presents Cool-Mem, a family of memory system architectures that integrate conventional memory system mechanisms, energy-aware address translation, and compiler-enabled cache disambiguation techniques, to reduce energy consumption in general-purpose architectures. The solutions provided in this article leverage on interlayer tradeoffs between architecture, compiler, and operating system layers. Cool-Mem achieves power reduction by statically matching memory operations with energy-eff ...

Keywords: Energy efficiency, translation buffers, virtually addressed caches

16 Data cache locking for higher program predictability
Xavier Vera, Björn Lisper, Jingling Xue
June 2003 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2003 ACM SIGMETRICS international conference on Measurement and modeling of computer systems**, Volume 31 Issue 1

Full text available: pdf(292.01 KB) Additional Information: full citation, abstract, references, citings, index terms

Caches have become increasingly important with the widening gap between main memory and processor speeds. However, they are a source of unpredictability due to their characteristics, resulting in programs behaving in a different way than expected.Cache locking mechanisms adapt caches to the needs of real-time systems. Locking the cache is a solution that trades performance for predictability: at a cost of generally lower performance, the time of accessing the memory becomes predictable.This pape ...

Keywords: data cache analysis, worst-case execution time

17 Session 5: An adaptive serial-parallel CAM architecture for low-power cache blocks
Aristides Efthymiou, Jim D. Garside
August 2002 **Proceedings of the 2002 international symposium on Low power electronics and design**

Full text available: pdf(151.38 KB) Additional Information: full citation, abstract, references, citings, index terms

There is an on-going debate about which consumes less energy: a RAM-tagged associative cache with an intelligent order of accessing its tags and ways (e.g. way prediction), or a CAM-tagged high associativity cache. If a CAM search can consume less than twice the energy of reading a tag RAM, it would probably be the preferred option for low-power applications. Based on memory traces --- which usually cause tag mismatch within the lower four bits --- a new serial CAM organisation is proposed which ...

Keywords: CAM, VLSI, asynchronous circuits, cache design, low energy, low power

18 Timing analysis and memory optimization for embedded systems: Associative caches in formal software timing analysis
Fabian Wolf, Jan Staschulat, Rolf Ernst
June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(222.32 KB) Additional Information: full citation, abstract, references, citings, index terms

Precise cache analysis is crucial to formally determine program running time. As cache simulation is unsafe with respect to the conservative running time bounds for real-time systems, current cache analysis techniques combine basic block level cache modeling with explicit or implicit program path analysis. We present an approach that extends instruction and data cache modeling from the granularity of basic blocks to program segments thereby increasing the overall running time analysis precision. ...

Keywords: cache analysis, embedded software, real-time, timing analysis

19 Disconnected operation for heterogeneous servers
Dorota M. Huizinga, Patrick Mann

February 1996 **Proceedings of the 1996 ACM symposium on Applied Computing**
Full text available: pdf(857.48 KB) Additional Information: full citation, references, citings, index terms

Keywords: disconnected operation, mobile computing

20 Cyclic dependence based data reference prediction
Chi-Hung Chi, Jun-Li Yuan, Chin-Ming Cheung
May 1999 **Proceedings of the 13th international conference on Supercomputing**
Full text available: pdf(1.51 MB) Additional Information: full citation, references, index terms

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